In re Patent Application of:
ROCHE
Serial No. **09/479,105**
Filing Date: **JANUARY 7, 2000**

REMARKS

Applicant would like to thank the Examiner for the thorough examination of the present application. The arguments supporting patentability of the claims are provided in detail below.

I. The Claims Are Patentable

Independent Claims 10, 19, 26 and 37 have been rejected over the Banno et al. patent. The present invention, as recited in independent Claim 10, for example, is directed to a microprocessor comprising an address bus, a data bus, a plurality of read and write accessible registers connected to the data bus, and an address decoder connected to the address bus for selecting the plurality of registers as a function of an address provided by the address bus.

The microprocessor further comprises a plurality of protection circuits connected between the address decoder and the plurality of registers. Each protection circuit is associated with a register to secure access thereto by blocking selection of the register after each resetting of the microprocessor. The protection circuit is released by a successive sending on the data bus N passwords proper to the register during N first operations for selection of the register, with $N \geq 1$. The selection of the associated register is effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor.

The protection circuits advantageously provide secure access to the read and write accessible registers after the microprocessor has been reset. Each protection circuit is released by a successive sending on the data bus N passwords

proper to the register during N first operations for selection of the register.

Independent Claim 19 is similar to independent Claim 10 except Claim 19 further recites that a register is blocked "during write access operations" after each resetting of the microprocessor. Independent Claim 26 is similar to independent Claim 10 but further recites that "at least two passwords are provided to each register."

Banno et al. is directed to a microcomputer having a read protection circuit for securing the contents of an internal memory. The internal program memory read protection circuit **12** is best illustrated in FIGS. 1 and 2. Reference is directed to column 4, lines 48-58 of Banno et al., which provides:

> "FIG. 2 shows an example of the detailed arrangement of the internal program memory read protection circuit **12**. The protection circuit **12** comprises an address decoder **12a**, a memory element **12b**, and an AND gate **12c**.
>
> The address decoder **12a** receives an address transferred from the address bus **15**, detects if the received address is present in the address space of the internal program memory **13**, and outputs the detection results."

When the address is present in the internal program memory **13**, a logic 1 is stored in the memory element **12b**, otherwise a logic 0 is stored. An instruction fetch signal is output from the instruction execution unit **11d**, and is also supplied to the memory element **12b**. In synchronization with

the supply timing of the instruction fetch signal to the memory element **12b**, the detection result output from the address decoder **12a** is stored in the memory element **12b**.

The output from the memory element **12b** and the output from the address decoder **12a** are input to the AND gate **12c**. A read inhibit signal is generated by the AND gate **12c** based upon whether the address is present in the internal program memory **13**.

In sharp contrast, independent Claim 10 recites that each protection circuit is associated with a register to secure access thereto by blocking selection of the register after each resetting of the microprocessor. Banno et al. fails to disclose that access to the internal program memory **13** is blocked after each resetting of the microprocessor. Instead, access to the internal program memory **13** may be made at any time as long as a read inhibit signal is not generated by the AND gate **12c**.

In addition, independent Claim 10 recites that each protection circuit is released by a successive sending on the data bus of N passwords proper to the register during N first operations for selection of the register. In sharp contrast, Banno et al. fails to disclose the exchange of passwords over the data bus, as best illustrated in FIG. 2. Instead, the internal program memory read protection circuit **12** is "released" based upon the output from the memory element **12b** and the output from the address decoder **12a**, which in turn is based upon whether the address is present in the internal program memory **13**.

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Therefore, the Applicant submits that independent Claim 10 is patentable over the Banno et al. patent. Independent Claims 19, 26 and 37 are similar to independent Claim 10, and it is submitted that Claims 19, 26 and 37 are also patentable over the Banno et al. patent. In view of the patentability of the independent claims as discussed above, it is submitted that their dependent claims, which recite yet further distinguishing features, are also patentable over the prior art. Thus, these dependent claims require no further discussion herein.

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CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 703-872-9306 to the Commissioner for Patents on this 20 day of December, 2004.